Customer No.: 31561
Application No.: 10/605,082
Docket No.: 10228-US-PA

REMARKS

Present Status of the Application

The Office Action rejected claims 9-16 under 35 U. S. C. 102(e) as being anticipated by Kwon (U.S. Publication No. 2004/0012081). Claims 9-11 were rejected under 35 U. S. C. 102(e) as being anticipated by Lin (U.S. Publication No. 2004/00029404). Claims 9-10, 12-13 and 15-16 were rejected under 35 U. S. C. 103(a) as being unpatentable over Kunimatsu et al. (US Patent 5,767,564) in view of Ractificar et al. (U.S. Publication No. 2003/0121958) and Nguyen et al. (US Patent 6,238,949). Claims 11 and 14 were rejected under 35 U. S. C. 103(a) as being unpatentable over Kuminatsu et al. in view of Ractificar et al. and Nguyen, and further in view of Lin (U.S. Patent No. 6,303,423). Applicants have amended claims 9 and 13 and have cancelled claim 10. After entry of the amendments and considering the following remarks, reconsideration and withdrawal of these rejections are respectfully requested.

Foreign Priority

Applicant respectfully submits an English translation of Taiwanese application No. 91137426 corresponding to this application for consideration of the foreign priority. Applicant claims foreign priority benefits of Taiwanese application No. 91137426 filed on December 26, 2002, and this application should be entitled to have the earlier filing date.

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Discussions of the 102 and 103 rejections

Claims 9-16 were rejected under 35 U. S. C. 102(e) as being anticipated by Kwon (U.S. Publication No. 2004/0012081). Claims 9-11 were rejected under 35 U. S. C. 102(e) as being anticipated by Lin (U.S. Publication No. 2004/00029404).

As noted by the Office Action, this application has claimed the foreign priority benefits of the corresponding Taiwanese application No. 91137426, filed on 12/26/2002. Upon submittal of its English translation, the cited references Kwon (U.S. Publication No. 2004/0012081) and Lin (U.S. Publication No. 2004/00029404) should be disqualified when compared with the priority date of this application.

Therefore, reconsideration and withdrawal of these 102 objections are respectfully requested.

Claims 9-10, 12-13 and 15-16 were rejected under 35 U. S. C. 103(a) as being unpatentable over Kunimatsu et al. (US Patent 5,767,564) in view of Ractificar et al. (U.S. Publication No. 2003/0121958) and Nguyen et al. (US Patent 6,238,949). Claims 11 and 14 were rejected under 35 U. S. C. 103(a) as being unpatentable over Kuminatsu et al. in view of Ractificar et al. and Nguyen, and further in view of Lin (U.S. Patent No. 6,303,423).

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Claims 9 and 13 have been amended to provide more descriptions for clarification

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according to the present invention. Applicants submit that independent claims 9 and 13 patently defines over the prior references for at least the reason that the cited art fails to disclose each and every feature as claimed in the present invention.

Amended independent claims clearly recite "a passive component with a plurality of terminal electrodes, wherein at least two terminal electrodes are respectively disposed at two ends of the passive component", and hence distinguish the present invention over the cited references.

Kunimatsu merely discloses providing a semiconductor element 2 on an insulating substrate 1 and a decoupling capacitor 3 placed on the element 2. The decoupling capacitor 3 is constituted by stacking a silicon substrate 4, a first thin metal (electrode) film 5, a dielectric film 6 and a second thin metal (electrode) film 7 in order. The conductor 8 is used to connect the first metal film 5 with the alloy 3A, while the first metal film 5 is not electrically connected to the second metal film 7.

Obviously, Kunimatsu fails to teach or suggest a passive component with terminal electrodes and at least two terminal electrodes being respectively disposed at two ends of the passive component.

As noted by the Office Action, Kunimatsu fails to teach a UBM layer and a bonding pad under solder block, and a plastic to encapsulate the die. The Office Action relied on Ratificar and Nguyen for teaching the lacking features and asserted that it is obvious to modify Kunimatsu's process with UBM layer and bonding pads, as well as using plastic

package.

Applicant respectfully disagrees with this assertion. The hindsight rationalization proposed by the Office Action is not once mentioned in Kunimatsu, Ratificar or Nguyen, and contrary to the teaching of these patents. The only suggestion to combine the various features from each patent comes from the applicant's specification and claims.

Because all the cited references fail to teach, suggest or disclose each and every feature of the present invention, and therefore they cannot possibly arrive at the claimed invention, as suggested by the Office Action. Accordingly, Applicants respectfully submits that independent claims 9 and 13 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims patently define over the prior art references as well.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : Sept. 24, 2004

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Application No.: 10/605,082
Docket No.: 10228-US-PA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	**Min-Lung Huang**
Application No.	:	**10/605,082**
Filed	:	**September 08, 2003**
Title	:	**METHOD OF ASSEMBLING PASSIVE COMPONENT**
Grp./Div.	:	**2812**
Examiner	:	**Tsai, H Jey**
Docket No.	:	**10228-US-PA**

STATEMENT BY TRANSLATOR UNDER 37 C.F.R. § 1.55

Assistant Commissioner for Patents
Alexandria, VA 22202

Commissioner:

I hereby declare that I translated the Taiwan patent Applicant No. 91137426 to English and a true and correct copy of the English-language translation is attached hereto.

I hereby confirm that the English translation enclosed herewith is an accurate translation of the Taiwan Patent Applicant no. 91137426 which was file on December 26, 2002.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date Sep. 24, 2004 **By** _____
Caroline Pao

TRANSLATION

Specification for Patent Application

I. Title: METHOD OF ASSEMBLING PASSIVE COMPONENT

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IV. ABSTRACT OF THE INVENTION

A method of assembling a passive component over the active surface of a die is provided. The method shortens the signal transmission path between the die and the passive component so that electrical performance of the die after packaging is improved. In addition, the transmission path and the number of contacts on the substrate for connecting the die and the passive component are reduced. With a reduction in transmission path, size of the substrate can be reduced. Furthermore, a plurality of passive components may be assembled onto the dies of a wafer in a single operation so that there is no need to assemble individual passive component over each packaging substrate.

(1) The representative drawing : Fig. 3

(2) Reference number of this representative drawing

100: substrate

102: the upper surface

104: bonding pad

106: conductive wires

108: contact pad

110: die

110a: active surface

110b: back surface

120: passive component

124: plastic materials

130: wire-bonded chip package

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V. DETAILED DESCRIPTION OF THE INVENTION

Field of Invention

The present invention relates to a semiconductor packaging technique. More particularly, the present invention relates to a method of assembling a passive component on the surface of a chip.

Description of Related Art

As semiconductor fabrication technique continues to progress, more precise and advance electronic devices are developed due to market demand. At present, popular techniques for packaging semiconductor devices include flip-chip assembly, integrated substrate design and passive component assembly.

Semiconductor production includes providing a wafer and forming highly integrated circuit on the active surface of the wafer. The active surface further includes a plurality of bonding pads thereon. Thereafter, the wafer is diced up into a plurality of dies. The die is subsequently wire-bonded or flip-chip-bonded to a carrier such as a lead frame or a substrate. The bonding pads on the die are redistributed to the periphery or a region over the active surface of the die through transmission circuits and contact points on the carrier.

To meet the requirements in an integrated circuit (IC) design, passive components are often attached to substrate surface using surface mount technology (SMT). Hence, the passive component is able to connect electrically with the die through the patterned circuit in the substrate. Ultimately, signals produced by the die are transmitted through the patterned circuit and passive component to an external electronic device.

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Note that the shorter the signal transmission path between the passive component and the die, the shorter will be the resistor-capacitor (RC) delay and hence raise overall electrical performance of the die and the passive component. Therefore, finding the shortest signal transmission path linking a passive component to the die is an important research issue.

SUMMARY OF THE INVENTION

Accordingly, one object of the present invention is to provide a method of assembling a passive component directly onto the surface of a die so that signal transmission path between the die and the passive component is shortened and corresponding transmission delay is reduced.

To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a method of assembling a passive component on a die with an active surface. The passive component has a plurality of electrodes located on the periphery and the die has a plurality of bonding pads on the active surface. The method of assembling the passive component onto the die includes the following steps. An under-bump-metallurgy (UBM) layer is formed over the bonding pads. A solder block is formed on the UBM layer. And, the terminal electrodes of the passive component are bounded to the solder block. Optionally, a patterned dielectric layer can be formed over the active surface with openings to expose the bonding pads. Optionally, a RDL can be formed to electrically couple to the bonding pads, or the UBM layer can further include the RDL.

This invention also provides chip package structure that comprises a substrate, a die, at least one under-bump-metallurgy layer, a plurality of solder blocks, a passive

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component, a plurality of conductive wires and a packaging plastic. The substrate has an upper surface. The die has an active surface and a back surface. The back surface of the die is in contact with the upper surface of the substrate. The active surface of the die is implemented with a plurality of boding pads thereon. The under-bump-metallurgy layer is positioned over the bonding pads. The solder blocks are placed above the under-bump-metallurgy layer. The electrodes of the passive component are bounded to the under-bump-metallurgy layer through the solder blocks. The conductive wires connect the die and the substrate together. The packaging plastic encloses the die, the passive component and the conductive wires. Optionally, a patterned dielectric layer can be included, wherein the patterned dielectric layer has openings to expose the bonding pads. Optionally, a RDL can be included to electrically couple to the bonding pads, or the UBM layer can further include the RDL.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

Figs. 1 and 2 are schematic sectional view showing the steps for assembling a passive component on a die according to one preferred embodiment of this invention. As shown in Fig. 1, a patterned dielectric layer 114 is formed on the active surface 110a of a die 110. Thereafter, photolithographic and etching processes are carried out to

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form openings 114a in the dielectric layer 114. The openings 114a are located in positions corresponding to the bonding pads 112 on the die 110. Thus, the openings 114a expose all the bonding pads 112. Here, the dielectric layer 114 is an option of the invention as an example, and is not the required elements or processes. An under-bump-metallurgy layer 116 is formed over each bonding pad 112 by conducting electroplating, sputtering and evaporation coating. The steps for forming the under-ball-metallurgy layers 116 include forming a metallic layer over the bonding pads 112 and the dielectric layer 114 globally and then patterning (through photolithographic and etching processes) the metallic layer. The under-bump-metallurgy layer 116 can have a multi-layered structure that includes a stack of different metallic layers.

As shown in Fig. 2, solder blocks 118 are inserted into the openings 114a above the under-ball-metallurgy layer 116 by dip coating or printing. The solder blocks 118 are fabricated using a material such as lead-tin alloy. Finally, a passive component 120 is bonded to the solder blocks 118. The passive component 120, such as a resistor, a capacitor or an inductor, has two ends each having at least one electrode 122. Each electrode 122 is bonded to one of the solder blocks 118. Through the solder blocks 118, the electrode 122 and the bonding pad 112 on the die 110 are electrically connected. To increase bonding strength between the electrode 122 and the solder blocks 118, an additional reflow process is preferably conducted to obtain the consequent chip structure 126 as shown in Fig. 2.

Fig. 3 is a sectional view of a wire-bonded chip package having an assembled passive component therein according to one preferred embodiment of this invention. As shown in Fig. 3, the upper surface 102 of the substrate 100 has a die 110. The die 110 has an active surface 110a and a corresponding back surface 110b. The back

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surface 110b of the die 110 is attached to the upper surface 102 of the substrate 100. The dielectric layer constituting the substrate 100 may be fabricated from a ceramic material or an organic material. The active surface 110a of the die 110 has a plurality of bonding pads 112. The bonding pads 112 can be electrically coupled to a re-distribution layer (RDL). As can be known by the skilled artisans, the RDL is used to re-redistribute the connection terminal pads of an IC to the proper positions for easy packaging. The use of RDL is optional and the RDL can be formed by an additional layer or formed by integrating in the UBM layer, wherein the UBM also provides the function of RDL. However, the RDL does not affect the features of the invention. Then, the bonding pads 112 are fabricated using aluminum or copper, for example. It should be noted that the passive component 120 (inside circle A) and the die 110 are assembled and electrically connected together through the bonding pad 112 on the active surface 110a.

According to the passive component assembling method and wire-bonded chip package as shown in Figs. 1, 2 and 3, passive components 120 may be assembled to the surface of a wafer before dicing the wafer into single dies. Thereafter, the dies are individually attached to a substrate 100 and enclosed to form a package as shown in Fig. 3. The process includes providing a wafer (containing many undiced dies) with a plurality of bonding pads 112 on the active surfaces 110a and then forming the dielectric layer 114, the under-bump-metallurgy layers 116 and the solder blocks 118 as described with reference to Figs. 1 and 2. Thereafter, the electrodes 122 of the passive components 120 are bonded to the respective solder blocks 118. Hence, the active surface 110a of the wafer (with undiced die 110 thereon) has a plurality of passive components thereon. Consequently, the wafer is diced to produce single dies.

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In Fig. 3, the die 110 is attached to the upper surface 102 of the substrate 100 with the bonding pad 104 on the die 110 electrically connected to the contact pad 108 on the substrate 100 through a conductive wire 106. Plastic materials 124 are injected to enclose the die 110, the passive component 120 and the conductive wires, thereby forming a wire-bonded chip package 130.

In summary, major advantages of the passive component assembling method according to this invention include:

1. A passive component is directly attached to the active surface of a die so that signal transmission path between the die and the passive component is shortened and corresponding transmission delay is reduced.
2. By attaching the passive component onto the active surface of a die directly, the number of transmission circuits and contact points in the substrate for connecting between the die and the passive component is reduced. Hence, size of the substrate can be reduced.
3. Passive components can be assembled to the active surface of a wafer in a single operation after complete fabrication of the wafer. This speeds up and simplifies the process of attaching a die to a substrate.

It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.

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BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

Figs. 1 and 2 are schematic sectional view showing the steps for assembling a passive component on a die according to one preferred embodiment of this invention.

Fig. 3 is a sectional view of a wire-bonded chip package having an assembled passive component therein according to one preferred embodiment of this invention.

REFERENCE NUMBER OF THE DRAWINGS

100: substrate

102: the upper surface

104: bonding pad

106: conductive wires

108: contact pad

110: die

110a: active surface

110b: back surface

112: bonding pads

114: dielectric layer

114a: openings

116: under-bump-metallurgy layers

118: solder block

120: passive component

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122: terminal electrodes

124: plastic materials

126: chip structure

130: wire-bonded chip package

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WHAT IS CLAIMED IS:

1. A method of assembling a passive component on a die, wherein the passive component has a plurality of terminal electrodes and the die has an active surface with a plurality of bonding pads thereon, the assembling method comprising:

(1) forming a patterned dielectric layer over the active surface if the die, wherein the dielectric layer includes a plurality of openings, exposing the bonding pads respectively;

(2) forming a plurality of under-bump-metallurgy (UBM) layers respectively over the bonding pads;

(3) forming a plurality of solder blocks between the openings and on the UBM layers; and

(4) bonding the terminal electrodes of the passive component to the solder blocks.

2. The assembling method of claim 1, wherein the die further comprises a re-distribution layer over the active surface of the die and the re-distribution layer forms the bonding pads.

3. The assembling method of claim 1, wherein in step (2), the step of forming the under-bump-metallurgy layer includes:

(a) blanketly forming a metallic layer over the bonding pads and the dielectric layer; and

(b) patterning the metallic layer to form the under-bump-metallurgy layer over the bonding pads.

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4. The assembling method of claim 3, wherein the step of blanketly forming the metallic layer includes one selected from the group consisting of electroplating, sputtering, and evaporation.

5. The assembling method of claim 3, wherein the metallic layer is a composite metallic layer.

6. The assembling method of claim 1, wherein the under-bump-metallurgy layer is a composite metallic layer.

7. The assembling method of claim 1, wherein step (4) includes positioning the terminal electrodes in contact with the solder block and performing a reflow operation so that the solder block is melted and bonded with the terminal electrodes.

8. A chip structure, comprising:

a die having an active surface and a back surface, wherein the active surface is implemented with a plurality of bonding pads;

a dielectric layer disposed on the active surface of the die, wherein the dielectric layer includes a plurality of openings exposing the bonding pads respectively;

a plurality of under-bump-metallurgy layers respectively disposed over the bonding pads;

a plurality of solder blocks respectively disposed between the opneings and above the under-bump-metallurgy layer; and

a passive component having a plurality of terminal electrodes, which are respectively coupled to the UBM layer through the solder blocks.

9. The chip structure of claim 8, wherein the die further comprises a re-distribution layer on the active surface of the die and the re-distribution layer forms the bonding pads.

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10. The chip structure of claim 8, wherein the under-bump-metallurgy layer is a composite metallic layer.

11. A chip package structure, at least comprising:

a substrate having an upper surface;

a die having an active surface and a back surface, wherein the back surface of the die is in contact with the upper surface of the substrate and the active surface is implemented with a plurality of bonding pads;

a dielectric layer disposed over the active surface of the die, wherein the dielectric layer includes a plurality of openings exposing the bonding pads;

a plurality of under-bump-metallurgy layers respectively disposed over the bonding pads;

a plurality of solder blocks disposed between the openings and on the under-bump-metallurgy layer;

a passive component with a plurality of terminal electrodes, wherein the terminal electrodes are coupled to the under-bump-metallurgy layer through the solder blocks;

a plurality of conductive wires electrically connecting the die and the substrate; and

a packaging plastic enclosing the die, the passive component, and the conductive wires.

12. The chip package structure of claim 11, wherein the die further comprises a re-distribution layer on the active surface of the die and the re-distribution layer forms the bonding pads.

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13. The chip package structure of claim 11, wherein the under-bump-metallurgy layer is a composite metallic layer.

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